

REMARKS

Claims 1-40 are pending. Claims 41-49 are canceled. Claims 1-4, 6-7, 10-14, 16-24, 26-28, and 30-40 are amended to correct grammatical and typographical errors, and to more particularly point out and distinctly claim Applicants' invention.

The Examiner rejected Claims 1-6, 8-26 and 28-40 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,765,260 ("Hung"). With respect to Claims 1-4, 6, 21-24 and 26, the Examiner states:

Regarding claims 1-4, 6, 21-24 and 26, Hung discloses in figs. 3G-3H an electrically erasable programmable memory device, comprising: a first semiconductor layer 200 doped with a first dopant in a first concentration (p-type); a second semiconductor layer 202, adjacent the first semiconductor layer 200, doped with a second dopant that has an opposite electrical characteristic than the first dopant (n-type), the second semiconductor layer having a top side; two spaced-apart diffusion regions 212/216 embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration (col. 6, lines 4-25), the two diffusion regions including a, first diffusion region 218a/218b and a second diffusion region 216, a first channel region defined between the first diffusion region 218a/218b and the second diffusion region 216; a floating gate 214a/214b, comprising a conductive material, disposed adjacent the first diffusion region 218a/218b and above the first channel region and separated therefrom by a first insulator region 212, the floating gate 214a/214b capable of storing electrical charge and having at least two lateral sides; and a control gate 208a/208b, comprising a conductive material, disposed laterally adjacent the floating gate 214a/214b and surrounding at least two sides of the floating gate (see fig. 6) and separated therefrom by a vertical insulator layer 212, the control gate 208a/208b being disposed above the first channel region and separated therefrom by a second insulator region 206a/206b.

Applicants respectfully traverse the Examiner's rejection. With respect to Claim 1, as amended, Claim 1 recites, in pertinent part, that the control gate and the floating gate share a planarized top surface:

... a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate being capable of storing electrical charge; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate and separated therefrom by a first vertical insulator layer, wherein the control gate is adjacent the second diffusion region and above the first channel region and separated therefrom by a second insulator region, and wherein the control gate and the floating gate share a planarized top surface.

(emphasis added)

This limitation and its benefits, which are taught in Applicants' Specification, for example, at Figures 2 and 3, and at paragraph [0027], as originally filed, are neither disclosed nor suggested by Hung. In fact, Hung teaches forming the floating gate by etching back a conformal conductive layer over a capping layer that covers the control gate (see, for example, Hung at col. 5, lines 41-65. Hung does not disclose a planarization step affecting the control gate and the floating gate. Thus, Applicants respectfully submit that Claim 1 and its dependent Claims 2-6 and 8-20 are each allowable over Hung.

With respect to independent Claim 21, Claim 21 recites that the control gate is adjacent the floating gate on at least on two sides of the floating gate:

a floating gate, comprising a conductive material, disposed adjacent the first diffusion region and above the first channel region and separated therefrom by a first insulator region, the floating gate capable of storing electrical charge; and

a control gate, comprising a conductive material, disposed laterally adjacent the floating gate on at least two sides of the floating gate and separated therefrom by a vertical insulator layer. the control gate being disposed above the first channel region and separated therefrom by a second insulator

region.

(emphasis added)

These limitations and their benefits, which are taught in Applicants' Specification, for example, at Figures 4 and 7, and at paragraphs [0025] and [0044], as originally filed, are also neither disclosed nor suggested by Hung. Contrary to the Examiner's contention, Hung's Figure 6 merely shows control gate 208b adjacent only on one side of floating gate 214b and control gate 208a also adjacent only on one side of floating gate 214a. Therefore, Applicants respectfully submit that Claim 21 and its dependent Claims 22-26 and 28-40 are each allowable over Hung. Reconsideration and allowance of Claims 1-6, 8-26 and 28-40 are therefore requested.

The Examiner rejected Claims 7 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Hung, in view of U.S. Patent 5,427,968 ("Hong"). The Examiner states:

Hung fails to disclose the first vertical insulator is an ONO structure. However, Hong teaches in col. 3, lines 63-68 that the vertical insulator layer 64 is formed of ONO (figs. 4c-4d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Hung by forming the ONO layer as taught by Hong since the material such as oxide, NO or ONO layer is recognized equivalent material for forming the dielectric layer in a semiconductor device.

Applicants respectfully traverse the Examiner's rejection. As Claims 7 and 27 depend from Claims 1 and 21 respectively, Claims 7 and 27 are allowable over Hung for the reasons already stated above with respect to their parent claims. Hong's teachings of forming an ONO layer do not cure the deficiencies of Hung. Therefore, Applicants submit that Claims 7 and 27 are each allowable over the combined teachings of Hung and Hong. Reconsideration and allowance of Claims 7 and 27 are therefore requested.

Fee Authorization: The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication to Deposit Account No. 50-2257.

For the reasons set forth above, all pending claims (i.e., Claims 1-40) are believed allowable. If the Commissioner has any questions, the Commissioner is respectfully requested to telephone Applicants' attorney at (408) 392-9250.

Respectfully submitted,



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